Izhikevich neuron implementation for accurate spiking neural network simulations in neuromorphic hardware

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***Abstract*—Simulating neural signaling dynamics necessitates a highly scalable and accurate neuromorphic computing platform. Although hardware platforms can perform precise operations in parallel at a large scale, the limits of computing element resources can still easily be reached. Hence, simplified solutions are being investigated to conserve computational resources. In contrast to highly simplified multiplier-less Izhikivich neuron-based platforms, this work explores the effects of the calculation time step on the spike interval accuracy using a variable precision model. The model was implemented in Xilinx Kintex FPGA and evaluated against a reference simulation revealing a difference in spike rate as large as 8.06% with conventionally used time step values.**

***Keywords*—spiking neural network, FPGA, neuromorphic computing**

I. Introduction

Spiking neural networks (SNN) have been demonstrated to be preferable for certain applications (e.g. object detection with neuromorphic vision sensors [1] and with automotive LiDAR [2]). Further, they can be feasible, if the underlying operations are executed using appropriate processing environments. Interconnected leaky integrate-and-fire neurons (LIF) implemented in digital architecture are widely adopted choice for large-scale SNNs with efficient resource utilization, however, for the purpose of exploring more complex firing dynamics the system needs to possess a higher level of biological realism. More realistic models capable of different firing patterns, such as the Izhikevich model [3], are selected to mimic the neuron's behaviour more closely at the expense of a higher computational complexity. Regardless of the processing scheme's plausibility, small numerical inaccuracies still appear when translating the model into a digital circuit, which can accumulate significant inaccuracy in spike intervals [4]. In this work, we incorporate a mechanism into the Izhikevich model to regulate the computational accuracy allowing to prioritize error reduction and evaluate the effects of the time step size.

II. Neuron model

A. Izhikevich neuron

In Izhikevich neuron model [3] the Hodgkin-Huxley neuron model [5] is reduced to a system of ordinary differential equations as follows:

$$\begin{cases} v' = 0.04v^2 + 5v + 140 - u + I \\ u' = a(bv - u), \end{cases} \tag{1}$$

where v represents the membrane potential, u is a membrane recovery variable, a sets the time scale for the recovery variable and b describes the sensitivity to subthreshold fluctuations. When the spike reaches a potential threshold the system is reset to an after-spike state accordingly:

$$v \geq V_{th}, \text{ then } \{v = c, u = u + d\}, \tag{2}$$

where parameters c and d describe the after-spike reset values of the membrane potential and the recovery variable. Contrary to unrealistically simple LIF model, this model is capable of reproducing spiking and bursting dynamics exhibited by cortical neurons.

B. Numerical solution

Euler's method [6] can be used to calculate approximations to the neuron model at any given value. Applying Euler's method to (1) gives the discrete-time equations for membrane potential and recovery variable values:

$$\begin{cases} v_{n+1} = v_n + \Delta t(0.04v_n^2 + 5v_n + 140 - u_n + I) \\ u_{n+1} = u_n + \Delta t a(bv_n - u_n). \end{cases} \tag{3}$$

The Euler method is known to be a first order-method, which means the local truncation error $e(\Delta t)$ is related to the step size as $e(\Delta t) = O(\Delta t^2)$ and the global truncation error $E(\Delta t)$ as $E(\Delta t) = O(\Delta t)$. Notably, the effect of the local errors is compounded as rounded values are used in subsequent calculations. In reality, fixed point round-off error also contributes to the global error, which is then no longer linear to Δt. Choosing a smaller step size will start increasing $E(\Delta t)$, when fixed point precision error is not sufficiently small compared to the step size. This effect needs to be recognized to determine the appropriate fixed point variable size and step size.

III. Digital circuit design

A. Fixed point operations

It is possible to reorder (3) by replacing the parameters, b, I with $b^* = \Delta t b$ and $I^* = \Delta t I$. In addition, multiplication with the factor $0.04\Delta t$ can be substituted with shift operation by selecting Δt such that the factor is exactly a power of two. While this limits the time step resolution, multiplications are

exact and increasingly smaller Δt values can be selected. The two calculation pipelines to be implemented becomes:

$$\begin{cases} v_{n+1} = v_n + v_n^2 \gg n + 5\Delta t v_n + 140\Delta t - u_n^* + I^* \\ u_{n+1} = u_n^* + a(b^* v_n - u_n^*), \end{cases} \tag{4}$$

where n is the number of places to shift v_n^2 and $\gg$ is the binary right shift operation. The remaining multiplying operations are left as is and implemented with hardware multipliers to conserve accuracy and flexibility for adjusting the parameters.

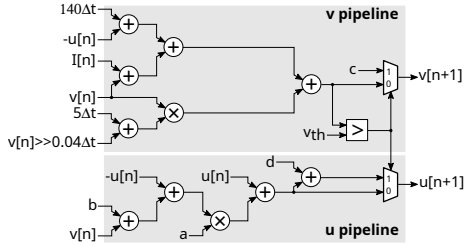

Fig. 1: Izhikevich neuron implementation using forward Euler method optimized for variable precision.

B. Implementation

The digital circuit implementation of (4) can be seen in Fig. 1. Since a single multiplier on the Xilinx Kintex FPGA is capable of 18-bit operations, the fixed point value of each multiplicand is constrained to 18-bit representation. In this case, a single multiplier is time multiplexed to conserve the DSP slice resources. Compared to other works, this solution gives the ability to adjust the time step at the cost of a higher computational latency. Each time step $\Delta t = 2^n/0.04$ can be used considering the number of shift operations n is an integer.

IV. Results

A regular spiking neuron with a time step of $0.781\,25\,\mathrm{ms}$ was implemented in Xilinx Kintex UltraScale KU115-2 FPGA and used for the fixed point implementation to produce waveforms in Fig. 2a. For comparison (3) are implemented in software with double precision floating point solver. In this case, both waveforms almost completely overlap suggesting the round-off error of 18-bit fixed point numbers is insignificant. However, reducing the time step in the floating point implementation in Fig. 2b exposes the effects of the step size on the global error. As a result, the interspike interval (ISI) starts to deviate from the expected interval with the same constant input current. Relative ISI error (RISI) quantifies the difference in spike intervals between fixed point and floating point calculations:

$$\mathrm{RISI}_{(\mathrm{FXP})}\% = \frac{\sum_{\mathrm{i=1}}^{\mathrm{N}} \frac{|\Delta \mathrm{t_i}|}{\mathrm{t_{DBLi}}}}{\mathrm{N}} * 100, \tag{5}$$

where N is the number of spikes measured, t_{DBL} is the time of spikes in double precision simulation and Δt_i is the difference in time of i-th spikes between fixed point and double precision simulations. Relative firing rate error (RFRE) evaluates the firing rate difference between fixed point and floating point calculations:

$$\mathrm{RFRE}_{(\mathrm{FXP})}\% = |\mathrm{FR_{FXP}} - \mathrm{FR_{DBL}}| * \mathrm{FR_{DBL}^{-1}} * 100, \tag{6}$$

where FR_{FXP} and FR_{DBL} are the fixed point and double precision firing rates $FR = ISI^{-1}$ at a constant postsynaptic current. A FR error as large as 8.06% can be observed with the time step of $0.781\,25\,\mathrm{ms}$.

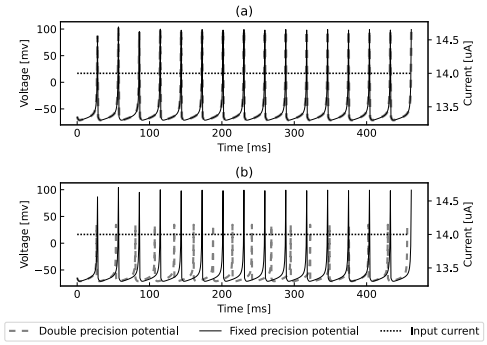

Fig. 2: Comparison between analytical double precision and proposed fixed point precision solution emphasizing the firing rate error: (**a**) Double and fixed precision $\Delta t = 0.781\,25\,\mathrm{ms}$, (**b**) Fixed precision $\Delta t = 0.781\,25\,\mathrm{ms}$ and double precision $\Delta t = 0.024\,414\,062\,5\,\mathrm{ms}$.

TABLE I: Fixed point firing interval errors ($I = 14\,\mu\mathrm{A}$, $a = 0.02$, $b = 0.2$, $c = -65$, $d = 6$, $V_{th} = 30\,\mathrm{mV}$) relative to the double precision solution with step size $\Delta t = 0.024\,414\,062\,5\,\mathrm{ms}$.

Time step, ms	***ISI,*** ms^{-1}	***RISI, %***	***RFRE, %***
7.812e-1	28.90625	7.5078	8.0554
3.906e-1	28.12500	4.9009	5.1271
1.953e-1	27.34375	2.1898	2.2116
9.765e-2	27.05078125	1.1470	1.1179
4.882e-2	26.904296875	0.6256	0.5701

V. Conclusions

This work demonstrates the considerable inaccuracies in Izhikevich neuron ISI that results from simplifications and a large time step in the model calculations. With the time step of $0.781\,25\,\mathrm{ms}$ conventionally used in other works, the FR of a regular spiking neuron implemented in digital logic is 8.06% slower than the reference simulation. For a model to match the reference simulation FR one of the proposed smaller time steps can be selected at the cost of a higher neuron latency.

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